REMARKS

Claims 32, 33, 36, 38-40, and 44-52 are pending in the present application. Claims 32-49 were presented for examination. Claims 34, 35, 37, and 41-43 have been cancelled and claims 50-52 have been added by amendment.

In the office action mailed February 3, 2005 (the "Office Action"), claims 45-49 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter applicants regard as the invention. Claims 32, 33, 34, and 38 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,987,628 to Von Bokern *et al.* (the "Von Bokern patent"). In the Office action, claim 35 was also rejected under 35 U.S.C. 103(a) as being unpatentably over the Von Bokern patent and U.S. Patent Nos. 5,809,228 to Langendorf *et al.* (the "Langendorf patent") and 6,151,658 to Magro (the "Magro patent"). Claims 36, 39-41, and 44 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Von Bokern patent and U.S. Patent No. 6,041,168 to Williams *et al.* (the "Williams patent"). Claim 37 was rejected under 35 U.S.C. 103(a) as being unpatentable over the Von Bokern patent and the Applicants' Admitted Prior Art (the "APA"). Claim 42 was rejected under 35 U.S.C. 103(a) as being unpatentable over the Von Bokern, Williams, and Magro patents. Claims 43 was rejected under 35 U.S.C. 103(a) as being unpatentable over the Von Bokern and Williams patents, and the APA.

With respect to the rejection of claims 45-49 under 35 U.S.C. 112, second paragraph, claim 45 has been amended to overcome the antecedent issues identified by the Examiner. It will be apparent from the amendments to claim 45, and the comments below, that the amendments were made independent of the cited references. None of previously mentioned amendments narrow or further limit the scope of the invention as recited by claim 45. Generally, the amendments make explicit what is implicit in the claim, add language that is inherent in the unamended claim, or merely redefine a claim term that is previously apparent from the description in the specification. Consequently, the amendments should not be construed as being "narrowing amendments," because these amendments were not made for a substantial reason related to patentability.

With respect to the rejection of claims 34, 35, 37, and 41-43, the Examiner's rejections are now moot in light of the cancellation of these claims.

As previously mentioned, claims 32, 33, 34, and 38 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Von Bokern patent.

Claim 32 is patentably distinct from the Von Bokern patent. The Von Bokern patent is directed to storing data that has been corrected through the use of an error-correction code ("ECC") at the location of the original corrupt data. As described in the Von Bokern patent, many memory systems include the use of ECC to maintain and check the integrity of stored data. However, although use of the ECC can correct corrupt data upon retrieval in response to a read command, the corrected data is not rewritten to the memory to store the corrected version. Since ECC is usually limited to correcting a single flipped bit in the data, correctable corrupt data that is stored may become un-correctable if another bit of the data flips. By writing the corrected data back to the memory, cumulative data errors that prevent correction through the use of ECC can be avoided, or at least mitigated.

The subsystem controller described in the Von Bokern patent includes ECC logic 39 and read-merge-write ("RMW") logic 41. As explained in the Von Bokern patent, when data is retrieved from a memory subsystem 14, the ECC logic determines whether the data is corrupted and corrects the data if necessary and if possible. The corrected data is provided to the read buffers to complete the read request. The data retrieved from the memory subsystem 14 is provided to the RMW logic 41 and stored in a RMW buffer 105 (Figure 7). Under the control of a memory access control logic 30, the RMW logic 41 performs either a partial write operation or a "scrub operation." In a partial write operation, the data in the RMW buffer 105 is merged with data from another write buffer before being written to the memory subsystem 14. For a scrub operation, the memory access control logic 30 issues RMW control signals to cause a corrected data value to be stored in the RMW buffer 105 and then steered through the multplexers without modification. The corrected data in the RMW buffer 105 is then written back to memory to the address supplied in the scrub request. A new ECC can also be generated so that the corrected data is written to memory with the new ECC. *See* col. 13, line 57-col. 14, line 35.

As further described in the Von Bokern patent, an advantage of the subsystem controller is that the scrub operation, that is, correcting corrupted data and writing the corrected data back to the memory subsystem 14, leverages the RMW logic that is already present in a conventional subsystem controller. *See* col. 14, lines 36-45. Noticeably missing from the description in the Von Bokern patent is the use of the RMW buffer 105 to store the corrected

data *and* merge the *corrected data* with data from another write buffer. The Von Bokern patent distinguishes the two operations. The RMW operation of merging data in the RMW buffer 105 with data from another write buffer is specifically described separately from the "scrub operation," where corrected data is stored in the RMW buffer 105 and then written back to the memory subsystem 14 under the control of the memory access control logic 30.

The Examiner has cited to col. 5, line 61-col. 6, line 4, col. 13, lines 57-65, and col. 14, lines 3-20 as describing the merging of corrected (i.e., modified) data with data from another write buffer. The description at col. 5, line 61-col. 6, line 4 is ambiguous at best, failing to describe merging corrected data with data from another write buffer. As described there, "Data read from memory may be merged with data from other write buffers and written back to memory via the data path labeled WRITE DATA." However, the next line suggests that separate from merging read data with data from another write buffer, "[i]n an embodiment discussed below, *corrected data* is buffered within the RMW logic 41 and then written back to the memory subsystem 14 at an address provided by the memory correction logic 35." *See* col. 5, line 65-col. 6, line 4 (emphasis added). The distinction between the RMW operation and the scrub operation is made more clear at col. 13, line 66-col. 14, line 34, which was cited in part by the Examiner. This description specifically separates the RMW operation and the scrub operation.

Another indication that the two operations are separate is the description at col. 9, lines 1-26, where one embodiment gives scrub requests priority over other requests, suggesting that writing corrected data back to the memory subsystem 14 is give priority and should be completed to the exclusion of other operations. Additionally, as described in the Von Bokern patent, handling the sequence of access commands is simplified by giving scrub operations priority because it can be assumed that the next access command issued after a scrub request corresponds to the scrub operation.

Claim 32 recites a method for accessing the embedded memory array included in a graphics processing system comprising reading data and an associated error correction code from a location corresponding to a memory address in the embedded memory array; storing the data at a buffer location in a buffer memory; storing the memory address; processing at least a portion of the data to provide modified data; receiving write memory addresses; and when writing the modified data to the embedded memory array in response to a write memory address matching the stored memory address, logically combining the stored data and the modified data

and storing the combined data at the buffer location, calculating a new error correction code based on the combined data in the buffer memory, and storing the combined data and the new error correction code to the location corresponding to the memory address in the embedded memory array.

The Von Bokern patent fails to disclose the combination of limitations recited by claim 32. For example, the Von Bokern patent fails to describe storing the data read from embedded memory, storing the memory address of the data, processing at least a portion of the data to provide modified data, logically combining the stored data and the modified data, calculating a new ECC, and storing the combined data to the location corresponding to the memory address from which the data was originally stored in embedded memory. As previously discussed, operation of the subsystem controller described in the Von Bokern patent is not analogous to the method recited in claim 32. The subsystem controller of the Von Bokern patent is not described as performing the RMW operation with corrected data. Moreover, the RMW buffer 105 is not analogous to the buffer memory recited in claim 32 since the RMW buffer 105 is not described as being configured as the buffer memory of claim 32.

For the foregoing reasons, claim 32 is patentably distinct from the Von Bokern patent. Claims 33 and 38, which depend from claim 32 are also patentably distinct from the Von Bokern patent based on their dependency from allowable base claim 32. Therefore, the rejection of claims 32, 33, and 38 under 35 U.S.C. 102(b) should be withdrawn.

As previously mentioned, claim 39 has been rejected as being unpatentable over the Von Bokern patent and the Williams patent.

Claim 39 recites a method for accessing an embedded memory array of a graphics processing system that includes reading first data and an associated error correction code from a first location corresponding to a first memory address in the embedded memory array; storing the first data at a first buffer location in a first buffer memory having a plurality of buffer locations for storing a plurality of data; substantially concurrent with the reading and storing of the first data in the first buffer memory, logically combining second data previously stored at a second buffer location in a second buffer memory with modified data, calculating a new error correction code based on the combined second data in the second buffer memory, and storing the combined second data and the new error correction code to a second location corresponding to a second memory address in the embedded memory array from which the second data was originally read.

The method further includes processing at least a portion of the first data to provide first modified data, reading third data from a third location corresponding to a third memory address in the embedded memory array, storing the third data at a third buffer location in the second buffer memory, and substantially concurrent with the reading and storing of the third data, logically combining the first data stored at the first buffer location in the first buffer memory with the first modified data, calculating a new error correction code based on the combined first data in the first buffer memory, and storing the combined first data and the new error correction code to the first location corresponding to the first memory address in the embedded memory array.

The combined teachings of the Von Bokern and Williams patents fail to teach or suggest the combination of limitations recited by claim 39. As with claim 32, the Von Bokern patent fails to describe the limitations for which the Examiner has cited the reference. For example, the Von Bokern patent does not describe more than one RMW buffer, which the Examiner has analogized to the memory recited in claim 39. The Von Bokern patent further fails to describe storing the first data at a first buffer location in a first buffer memory having a plurality of buffer locations for storing a plurality of data. The Examiner has cited the Williams patent as teaching interleaving multiple memory sections of a FIFO during ECC checking and correcting data retrieved from a hard drive. That is, while data is being written to a first memory section, ECC operations are being performed on data stored in a second memory section, and data that has already been corrected is in a third memory section. Even if it is assumed that the Examiner's characterization of the Williams patent is accurate, the teachings do not make up for the deficiencies of the Von Bokern patent previously described.

For the foregoing reasons, claim 39 is patentable over the Von Bokern patent in view of the Williams patent. Claims 40 and 44, which depend from claim 40 are similarly patentable based on their dependency from allowable base claim 39. Therefore, the rejection of claims 39, 40, and 44 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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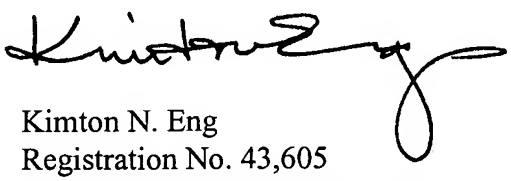

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